

**IN THE CLAIMS**

(1) Please cancel Claims 14-23 and 33-42.

1 1. (original) A parallel pattern detection engine (PPDE) integrated circuit (IC) for  
2 detecting one or more patterns in a sequence of input data comprising:

3 an input/output (I/O) interface for coupling data into and out of the PPDE;

4 M processing units (PUs), each of the M PUs having compare circuitry for  
5 comparing each of the sequence of input data to a pattern stored in each of the M PUs  
6 and generating a compare output, wherein an address pointer selecting the pattern in each  
7 of the M PUs is modified in response to a logic state of the compare output and an  
8 operation code stored with the pattern;

9 an input bus for coupling the sequence of input data to each of the M PUs in  
10 parallel;

11 an output bus coupled to the I/O interface for sending output data to the I/O  
12 interface;

13 control circuitry coupled to the I/O interface and coupling control data on a  
14 control data bus and identification (ID) on an ID bus to each of the M processing units;

15 ID selection circuitry for selecting a match ID from ID data identifying the M PUs  
16 in response to a pattern match signal and match mode data, wherein the match ID and  
17 match data corresponding to the match ID are saved in a temporary register as the output  
18 data; and

19 cascade circuitry coupled from each of the M PUs to one or more adjacent PUs  
20 within the M PUs for selectively coupling chain data between one or more groups of two  
21 or more adjacent PUs selected from the M PUs in response to the control data.

1 2. (original) The PPDE of claim 1 further comprising an input buffer coupled to the I/O  
2 interface for receiving and writing input data as parallel data at a write address.

1 3. (original) The PPDE of claim 2 further comprising a multiplexer coupled to the input  
2 bus and the input buffer for sequentially coupling single data from the input buffer data to  
3 the input bus, wherein parallel data are selected using a read address.

1 4. (original) The PPDE of claim 1 further comprising an output buffer coupled to the  
2 output bus and to the temporary register for receiving and writing output data to the  
3 output buffer at a write address and coupling output data to the output bus corresponding  
4 to a read address.

1 5. (original) The PPDE of claim 1, wherein each of M processing units (PUs) has an ID  
2 register for storing a unique ID sent from the control circuitry.

1 6. (original) The PPDE of claim 1, wherein each of M processing units (PUs) has a  
2 control register for storing the match mode data, wherein the match mode data  
3 determines criteria for generating the match signal and the match data.

1 7. (original) The PPDE of claim 1, wherein each of the M PUs has a memory register  
2 array for storing a sequence of the pattern and corresponding operation codes addressed  
3 by an address register indexed by the address pointer.

1 8. (original) The PPDE of claim 1, wherein the cascade circuitry enables the stored  
2 patterns of two or more PUs to be chained together as a single pattern using the chain  
3 data.

1 9. (original) The PPDE of claim 9, wherein the chain data inhibits indexing the pointer  
2 of one PU until an adjacent PU coupled with the cascade circuitry has compared a last  
3 pattern to an input data.

1 10. (original) The PPDE of claim 1, wherein the compare circuitry in each of the M PUs  
2 completes a compare of an input data to a selected pattern and generates a compare  
3 output and modifies the address pointer in the same cycle of a clock signal.

1 11. (original) The PPDE of claim 1, wherein the match mode data for each of the M PUs  
2 sets a match mode comprising:

3 an exact match mode, wherein a pattern match indicates that the sequence of  
4 pattern matches a sequence of input data exactly,

5 a longest match mode wherein a pattern match indicates that a particular sequence  
6 of pattern corresponding to the match ID has the largest number of data in a sequence  
7 that compared to a sequence of data in the sequence of input data wherein the match data  
8 indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular  
10 sequence of pattern bytes corresponding to the match ID has the largest number of data  
11 that compared in a broken sequence that compared to a broken sequence of input data,  
12 wherein the match data indicates the value of the largest number; and

13           a fuzzy match mode, wherein a pattern match indicates that a particular sequence  
14 of pattern corresponding to the match ID has the closet match to the sequence of input  
15 data as determined by a distance value, wherein the match data indicates the distance  
16 value.

1       12. (original) The PPDE of claim 1, wherein the operation codes are selected from a set  
2 of operation codes comprising:

3           a match operation code indicating that the address pointer is incremented if the  
4 compare output is a logic one and the address pointer is reloaded to its initial value if the  
5 compare output is a logic zero;

6           an inverse operation code indicating that the address pointer is to be incremented  
7 if the compare output is a logic zero and the address pointer is reloaded to its initial value  
8 if the compare output is a logic one;

9           a wildcard operation code indicating that the address pointer is incremented if the  
10 compare output is a logic zero or a logic one;

11          a multiple wild card operation code indicating that the address pointer is to be  
12 held if the compare output is a logic zero otherwise the address pointer is incremented;  
13 and

14          a last operation code indicating that the address pointer is frozen until the  
15 matching process receives a reset if the compare output is a logic one and the address  
16 pointer is reloaded to its initial value if the compare output is a logic zero.

1 13. (original) The PPDE of claim 1, wherein bits of the selected pattern are masked by a  
2 mask data stored in a mask register when the selected pattern is compared to an input  
3 data, the mask data indicating which bits of the selected pattern are not compared.

Claims 14-23 (Canceled)

1 24. (original) A data processing system comprising:

2 a central processing unit (CPU);

3 a random access memory (RAM);

4 one or more parallel pattern detection engines (PPDEs); and

5 a bus coupling the CPU, RAM, and the one or more PPDEs, wherein each of the  
6 PPDEs has an input/output (I/O) interface for coupling data into and out of the PPDE;

7 M processing units (PUs), each of the M PUs having compare circuitry for  
8 comparing each of the sequence of input data to a pattern stored in each of the M PUs  
9 and generating a compare output, wherein an address pointer selecting the pattern data in  
10 each of the M PUs is modified in response to a logic state of the compare output and an  
11 operation code stored with the pattern data;

12 an input bus for coupling the sequence of input data to each of the M PUs in  
13 parallel;

14 an output bus coupled to the I/O interface for sending output data to the I/O  
15 interface;

16 control circuitry coupled to the I/O interface and coupling control data on a  
17 control data bus and identification (ID) on an ID bus to each of the M processing units;

18 ID selection circuitry for selecting a match ID from ID data identifying the M PUs  
19 in response to a pattern match signal and match mode data, wherein the match ID and  
20 match data corresponding to the match ID are saved in a temporary register as the output  
21 data; and

22 cascade circuitry coupled from each of the M PUs to one or more adjacent PUs  
23 within the M PUs for selectively coupling chain data between one or more groups of two  
24 or more adjacent PUs selected from the M PUs in response to the control data.

1 25. (original) The data processing system of claim 24, wherein each of M processing  
2 units (PUs) has an ID register for storing a unique ID sent from the control circuitry.

1 26. (original) The data processing system of claim 24, wherein each of the M PUs has a  
2 memory register array for storing a sequence of the pattern and corresponding operation  
3 codes addressed by an address register indexed by the address pointer.

1 27. (original) The data processing system of claim 24, wherein the cascade circuitry  
2 enables the stored patterns of two or more PUs to be chained together as a single pattern  
3 using the chain data.

4 28. (original) The data processing system of claim 27, wherein the chain data inhibits  
5 indexing the pointer of one PU until an adjacent PU coupled with the cascade circuitry  
6 has compared a last pattern to an input data.

1 29. (original) The data processing system of claim 24, wherein the compare circuitry in  
2 each of the M PUs completes a compare of an input data to a selected pattern and

3 generates a compare output and modifies the address pointer in the same cycle of a clock  
4 signal.

1 30. (original) The data processing system of claim 24, wherein the match mode data for  
2 each of the M PUs sets a match mode comprising:

3 an exact match mode, wherein a pattern match indicates that the sequence of  
4 pattern matches a sequence of input data exactly;

5 a longest match mode wherein a pattern match indicates that a particular sequence  
6 of pattern corresponding to the match ID has the largest number of data in a sequence  
7 that compared to a sequence of data in the sequence of input data wherein the match data  
8 indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular  
10 sequence of pattern corresponding to the match ID has the largest number of data that  
11 compared to a broken sequence of input data, wherein the match data indicates the value  
12 of the largest number; and

13 a fuzzy match mode, wherein a pattern match indicates that a particular sequence  
14 of pattern corresponding to the match ID has the closet match to the sequence of input  
15 data as determined by a distance value, wherein the match data indicates the distance  
16 value.

1 31 (original) The data processing system of claim 30, wherein the operation codes are  
2 selected from a set of operation codes comprising:

3 a match operation code indicating that the address pointer is incremented if the  
4 compare output is a logic one and the address pointer is reloaded to its initial value if the  
5 compare output is a logic zero;

6 an inverse operation code indicating that the address pointer is to be incremented  
7 if the compare output is a logic zero and the address pointer is reloaded to its initial value  
8 if the compare output is a logic one;

9 a wildcard operation code indicating that the address pointer is incremented if the  
10 compare output is a logic zero or a logic one;

11 a multiple wildcard operation code indicating that the address pointer is to be held  
12 if the compare output is a logic zero otherwise the address pointer is incremented; and

13 a last operation code indicating that the address pointer is frozen until the  
14 matching process receives a reset if the compare output is a logic one and the address  
15 pointer is reloaded to its initial value if the compare output is a logic zero.

1 32 original) The data processing system of claim 30, wherein bits of the selected pattern  
2 are masked by a mask data stored in a mask register when the selected pattern is  
3 compared to an input data, the mask data indicating which bits of the selected pattern are  
4 not compared.

Claims 33-42 (Canceled)